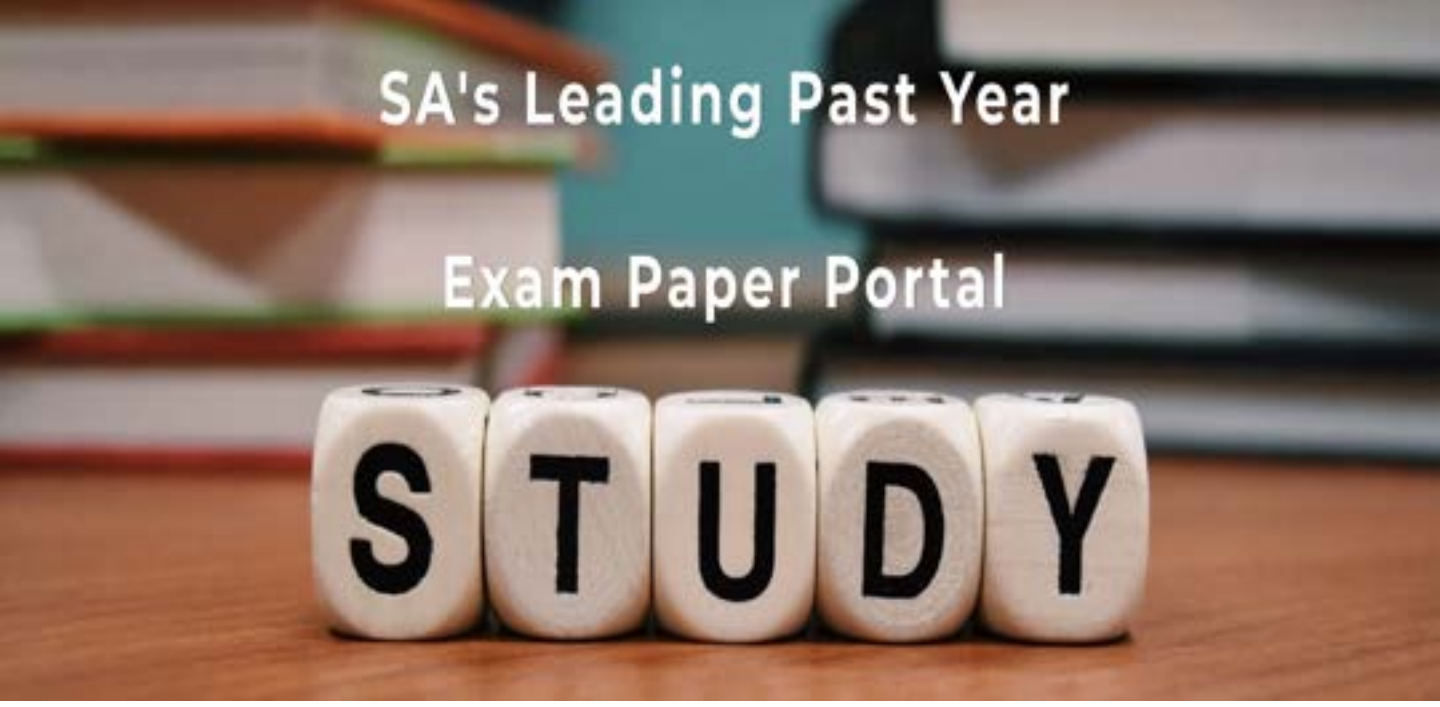

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GRADE 12

ELECTRICAL TECHNOLOGY: ELECTRONICS

NOVEMBER 2020

MARKING GUIDELINES

MARKS: 200

These marking guidelines consist of 17 pages.

INSTRUCTIONS TO THE MARKERS

1. All questions with multiple answers imply that any relevant, acceptable answer should be considered.

2. Calculations:

   2.1 All calculations must show the formulae.

   2.2 Substitution of values must be done correctly.

   2.3 All answers MUST contain the correct unit to be considered.

   2.4 Alternative methods must be considered, provided that the correct answer is obtained.

   2.5 Where an incorrect answer could be carried over to the next step, the first answer will be deemed incorrect. However, should the incorrect answer be carried over correctly, the marker has to re-calculate the values, using the incorrect answer from the first calculation. If correctly used, the candidate should receive the full marks for subsequent calculations.

3. This memorandum is only a guide with model answers. Alternative interpretations must be considered and marked on merit. However, this principle should be applied consistently throughout the marking session at ALL marking centres.

QUESTION 1: OCCUPATIONAL HEALTH AND SAFETY

1.1 Any article or part thereof which is manufactured, provided or installed ✓in the interest of the health or safety of any person. ✓ (2)

1.2 Your right to fair labour practices. ✓
Your right to work reasonable hours.
Your right to belong to a trade union.
Your right to earn a living wage.
Your right not to be discriminated against. (1)

1.3
- If a person dies. ✓
- A major incident. ✓
- An incident where the health and safety of any person has been/was endangered. (2)

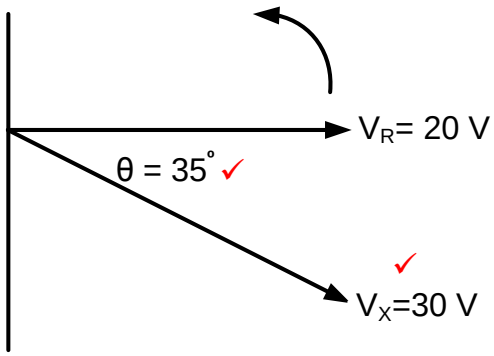
1.4
- To dismiss an employee without due process. ✓
- To reduce the rate of remuneration without due process. ✓
- Alter the terms of conditions of his/her employment to terms of conditions that is less favourable to him/herself. ✓
- Harassment and verbal abuse.
- Alter position relative to other people.
- Treat employees unfair because of race.

NOTE: If a learner mentions only a violation of rights 1 mark will be awarded. Duplicate mentioning of rights will not be awarded. (3)

1.5 In an emergency it can be pushed and it would immediately cut all electric power ✓ to all the equipment, stopping them,✓ thus making the workshop safe. (2)
[10]

QUESTION 2: RLC CIRCUITS

2.1 2.1.1 If V_X lags V_R by 35°



(2)

2.1.2 The voltages represent an RC circuit ✓ because, V_R is always in phase with I_T and V_X lags V_R by 35°. ✓
Because V_R is in phase with I_T and V_X is lagging V_R, thus proving that the circuit is predominantly capacitive as I_T leads V_X. (2)

2.2 2.2.1 $X_L = 2 \times \pi \times f \times L$ ✓
$= 2 \times \pi \times 60 \times 20 \times 10^{-3}$ ✓
$= 7{,}54\ \Omega$ ✓

(3)

OR

$X_L = \frac{V_L}{I_T}$

$X_L = \frac{49}{6.5}$

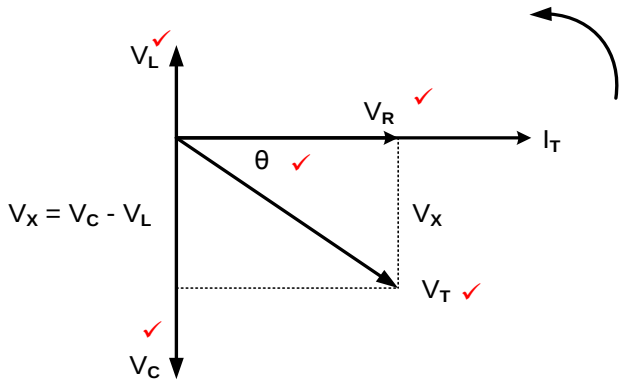
$X_L = 7{,}54\ \Omega$

2.2.2 $V_C = I \times X_C$ ✓
$= 6{,}5 \times 25$ ✓
$= 162{,}5\ V$ ✓

(3)

2.2.3 The voltage is lagging, ✓ because the capacitive reactance is greater than the inductive reactance (V_C is greater than V_L). ✓ (2)

2.2.4



(5)

NOTE: 5 marks, 1 mark for each correct label of which V_L, V_C and V_R are priority marks and thereafter any other two correct labels.

2.3 2.3.1 Phasor diagram of a parallel RLC✓ circuit at resonance. ✓ (2)

2.3.2 The voltage drop across the components in a parallel circuit is the same, ✓ hence the voltage is used as the reference. (1)

OR

The applied voltage is common across all components.

2.3.3 In a parallel resonant circuit impedance is at maximum, ✓ and the total current is at minimum. ✓ (2)

OR

The relationship between impedance and current in a parallel RLC circuit is inversely proportional.

2.4 2.4.1

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad ✓$$

$$= \frac{1}{2\times 3{,}142\sqrt{300\times10^{-3}\times150\times10^{-6}}} \quad ✓$$

$$= 23{,}73\ \text{Hz} \quad ✓$$

(3)

2.4.2

$$Q = \frac{1}{R}\times\sqrt{\frac{L}{C}} \quad ✓$$

$$= \frac{1}{20}\times\sqrt{\frac{300\times10^{-3}}{150\times10^{-6}}} \quad ✓$$

$$= 2{,}24 \quad ✓$$

(3)

OR

If candidates calculate X_L or Xc they can use the following formulae:

$X_L = 2\pi fL$

$X_L = 2\pi(23{,}73)(300\times10^{-3})$

$X_L = 44{,}73\ \Omega$

$Q = \frac{XL}{R}$ $\quad$ $Q = \frac{Xc}{R}$

$Q = \frac{44.73}{20}$ $\quad$ $Q = \frac{44.73}{20}$

$Q = 2{,}24$ $\quad$ $Q = 2{,}24$

2.4.3 $Z = 20\ \Omega$ ✓

$Z = R$ at resonance ✓

(2)

2.4.4
$$C = \frac{1}{4 \times \pi^2 \times L \times fr^2}$$ ✓
$$= \frac{1}{4 \times 9{,}87 \times 300 \times 10^{-3} \times 4 \times 10^6}$$ ✓
$$= 2{,}111 \times 10^{-8} F$$ ✓
$$= 21{,}11 \text{ nF}$$

(3)

OR

$$C = \frac{1}{(2\pi f_r)^2 \times L}$$
$$= \frac{1}{(2 \times 3{,}14 \times 2000)^2 \times 300 \times 10^{-3}}$$
$$= 2{,}113 \times 10^{-8} F$$
$$= 21{,}13 \text{ nF}$$

For resonance. Calculating X_L first and then since $X_L = X_C$

$$X_L = 2\pi fL$$
$$= 2\pi(2000)(300 \times 10^{-3})$$
$$= 3769{,}91\ \Omega$$
$$C = \frac{1}{2\pi fXC}$$
$$= \frac{1}{2\pi(2000)(3769{,}91)}$$
$$= 21{,}11 \text{ nF}$$

2.5. 2.5.1 Q_1 ✓ (1)

2.5.2 Reading the values from the graph where f_1 = 30000 Hz and f_2 = 35000 Hz the following can be deduced:

$$f_r = \frac{f_1 + f_2}{2}$$ ✓
$$= \frac{30000 + 35000}{2}.$$ ✓
$$= 32500 \text{ Hz}$$ ✓
$$= 32{,}5 \text{ kHz}$$

(3)

NOTE: If the candidate deduced the value 32,5 kHz directly from the graph, full marks will be awarded.

Because the incorrect formula was provided on the formula sheet, the following calculation will be accepted.

$$f_r = \frac{f2 - f1}{2}$$
$$= \frac{35000 - 30000}{2}$$
$$= 2500\ Hz$$

2.5.3 Deducing the indicated bandwidth of Q_1 from the graph as 35 kHz - 30 kHz the candidate will be able to calculate as follows:

$$BW = f_2 - f_1$$
$$= 35000 - 30000$$
$$= 5000\,Hz$$
$$BW = \frac{f_r}{Q}$$
$$Q = \frac{f_r}{BW}$$
$$= \frac{32500}{5000}$$
$$= 6,5$$

✓ ✓ ✓

OR

$$BW = \frac{f_r}{Q} \quad \text{and} \quad BW = (f_2 - f_1)$$
$$(f_2 - f_1) = \frac{f_r}{Q}$$
$$Q = \frac{f_r}{(f_2 - f_1)}$$
$$= \frac{32500}{(35000 - 30000)}$$
$$= 6,5$$

(3)
[40]

QUESTION 3: SEMICONDUCTOR DEVICES

3.1 3.1.1 A – Source ✓
B – Gate ✓
C – Drain ✓ (3)

3.1.2 N-type ✓ (1)

3.1.3 If the voltage on terminal B is 0 V, no current will flow between terminals A and C. ✓ (1)

3.1.4 A - Enhancement mode N-channel MOSFET ✓
C - P-channel JFET ✓
E - Depletion mode P-channel MOSFET ✓ (3)

3.2 Negative resistance is a characteristic of the UJT when it is triggered on, the current through the emitter terminal of the UJT rises ✓ while its potential falls. ✓
Negative resistance is when the UJT is triggered 'on' current floods into the lower base region and as the resistance falls, current through the bar rises. At the same time, the potential on the emitter terminal is pulled down. (2)

3.3 3.3.1 The Darlington pair is able to deliver very high output currents ✓ to drive a load from very small input base currents. ✓

Low output impedance to drive the output along long signal cable runs.
Very high input impedance in order to not pull / load down the preceding input stage. (2)

3.3.2 A BJT transistor normally needs 0,6 V to 0,7 V across its base emitter terminals to operate. ✓ The Darlington pair consists of two BJT transistors ✓ who's base emitter terminals are connected in series, ✓ therefore the Darlington pair will need a V_{BE} voltage from 1,2 to 1,4 V to operate. (3)

3.4 3.4.1 Infinite open loop gain. ✓
Infinite input impedance. ✓
Zero output impedance.
Infinite bandwidth.
Common mode rejection ratio. (2)

3.4.2 The Op-amp is ideal for amplifying AC voltages because of its dual voltage supply ✓ which allows the output terminal to rise and fall above and below zero volts. ✓ (2)

3.5 3.5.1 Point 'X' is known as virtual ground because both inputs have the same potential ✓ and the non-inverting input is connected to 0 V (ground) ✓ (2)

3.5.2
$$V_{OUT} = V_{IN} \times \left(-\frac{R_F}{R_{IN}} \right) \quad \checkmark$$

$$R_F = -\frac{V_{OUT}}{V_{IN}} \times R_{IN} \quad \checkmark$$

$$= -\frac{8}{0,4} \times 1,8 \times 10^3$$

$$= 36 \times 10^3 \Omega \quad \checkmark$$

$$= 36 \text{ k}\Omega$$

(3)

NOTE: The minus relates to the inverting function of the amplifier and is ignored for the resistive value of a resistor cannot be negative.
-36 kΩ is also accepted as correct.

3.6 3.6.1 Controlling the positioning of a servo device. ✓
Any timing application. (1)

3.6.2 Switch. ✓ (1)

3.6.3 Comparator 1 compares the upper voltage set up by the three 5 kΩ resistors at ⅔ of the supply voltage ✓ to the threshold voltage on pin 6. ✓
Comparator 2 compares the lower voltage set up by the three 5 kΩ resistors at ⅓ of the supply voltage ✓ to the trigger voltage on pin 2. ✓ (4)
[30]

QUESTION 4: SWITCHING CIRCUITS

4.1 The astable multivibrator has no external trigger input. ✓
The bistable multivibrator makes use of external trigger inputs. ✓ (2)

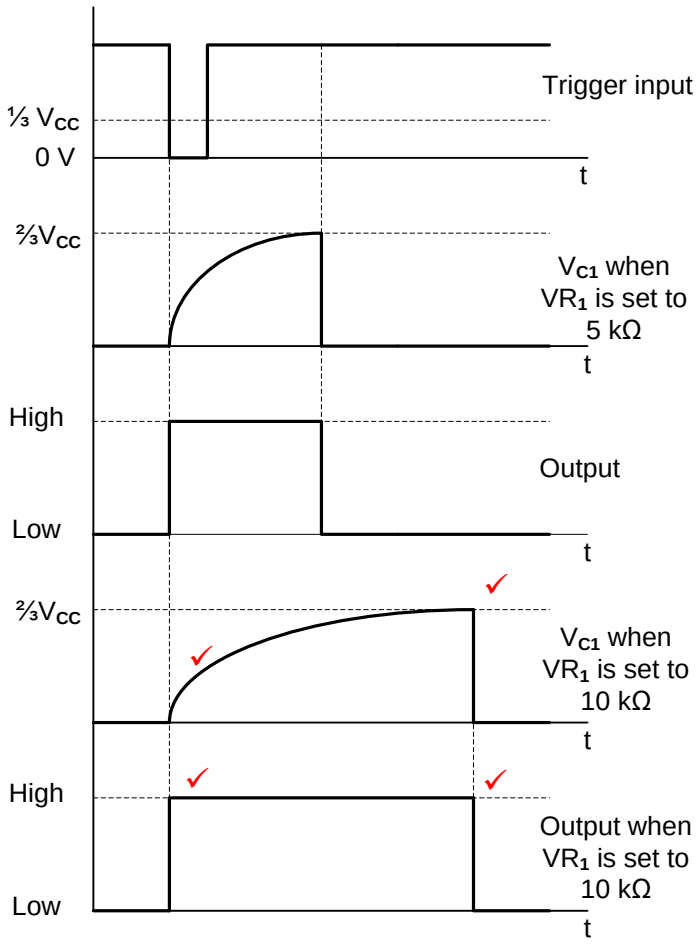
4.2 4.2.1 Astable multivibrator. ✓ (1)

4.2.2
- If point A is low it causes the Op-amp to saturate and its output to rise to +12 V. ✓
- This raises the potential across the voltage divider pair R_1 and R_2, making point B more positive than point A. ✓
- With the output voltage high, it induces the capacitor to charge towards +12 V through resistor R_F, gradually increasing the voltage at point A. ✓
- When the voltage at point A becomes more positive than the voltage at point B, the Op-amp immediately saturates in the opposite direction with its output falling to -12 V. ✓
- This forces the capacitor to discharge (or charge towards -12 V) through resistor R_F, decreasing the voltage at point A. ✓
- When the voltage at point A falls below that of point B, the Op-amp saturates back to +12 V and the process repeats itself. ✓ (6)

4.2.3 The frequency of the multivibrator can be increased by either decreasing ✓ the value of R_F or C_1. ✓ (2)

4.3 4.3.1 Capacitor C_2 removes any unwanted noise ✓ from the supply that might affect the timer operation. ✓ (2)

4.3.2

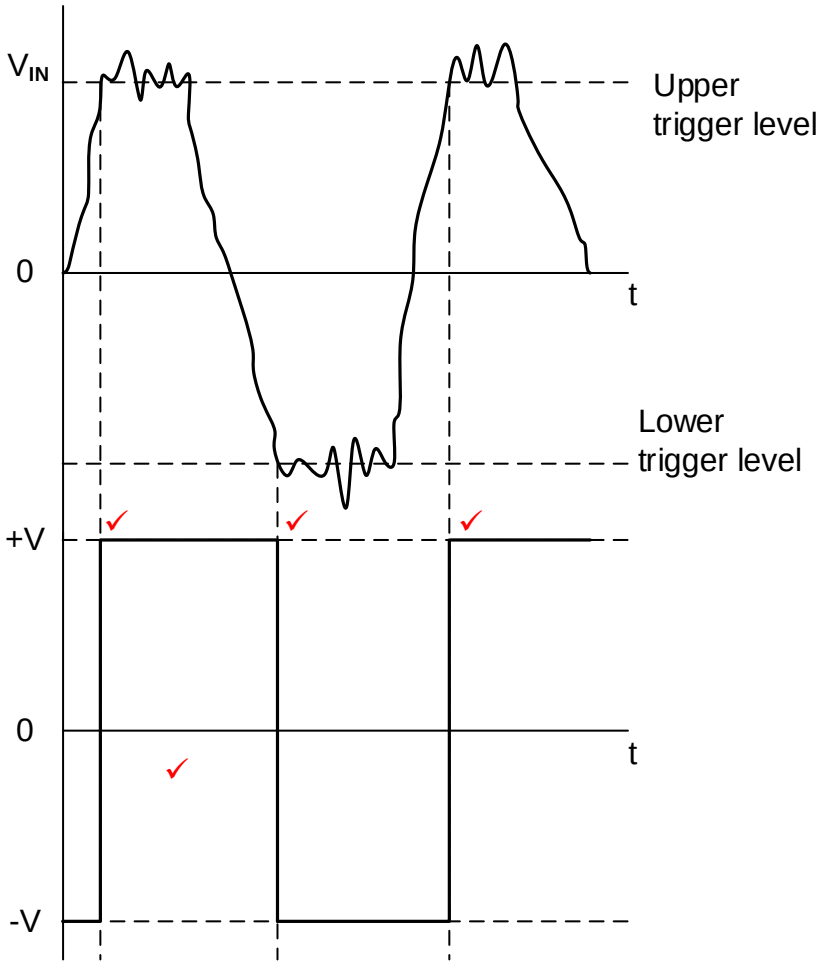


NOTE: 2 marks for the correct charging cycle of the capacitor
2 marks for the correct output signal. (4)

4.3.3 LED 2 will be ON ✓ because the output of the 555 IC goes high ✓ when the trigger switch is pressed, forward biasing LED 2 ✓ and reverse biasing LED 1. (3)

4.4 4.4.1 This is a closed loop mode ✓ Op-amp circuit because R_F creates a positive feedback loop from the output to the non-inverting input. ✓ (2)

4.4.2



NOTE: 1 mark for each correct trigger point.
1 mark for the correct orientation. (4)

4.4.3 The trigger voltage levels can be adjusted by changing ✓ the value of either R_F ✓ or R_1. (2)

4.5 4.5.1 Coupling capacitor ✓ used to pass the desired AC signals from the input and block unwanted DC signals. (1)

4.5.2

$$V_{OUT} = -\left(V_1 \times \frac{R_F}{R_1} + V_2 \times \frac{R_F}{R_2}\right) \quad ✓$$

$$= -\left(0{,}5 \times \frac{10000}{2000} + 0{,}2 \times \frac{10000}{500}\right) \quad ✓$$

$$= -6{,}5\ \text{V} \quad ✓$$

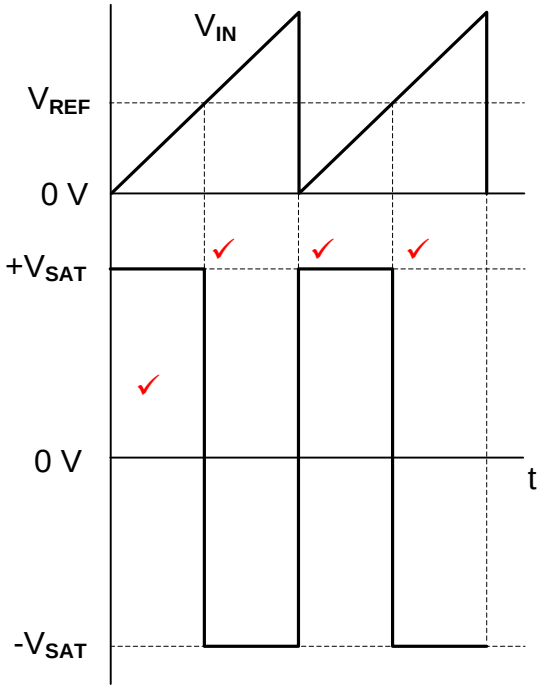
(3)

4.5.3 This amplifier is connected to a dual or split supply. ✓ The +12 V supply allows for the amplification of all positive signals ✓ and the -12 V supply allows for the amplification of all negative signals. ✓ (3)

4.5.4 If switch S1 is open, the output voltage will decrease, ✓ because input V_1 is disconnected and will not be added and only V_2 will be reflected on the output. ✓ (2)

4.6 4.6.1 Inverting ✓ comparator. ✓ (2)

4.6.2



NOTE: 1 mark for each correct trigger point.
1 mark for correct orientation. (4)

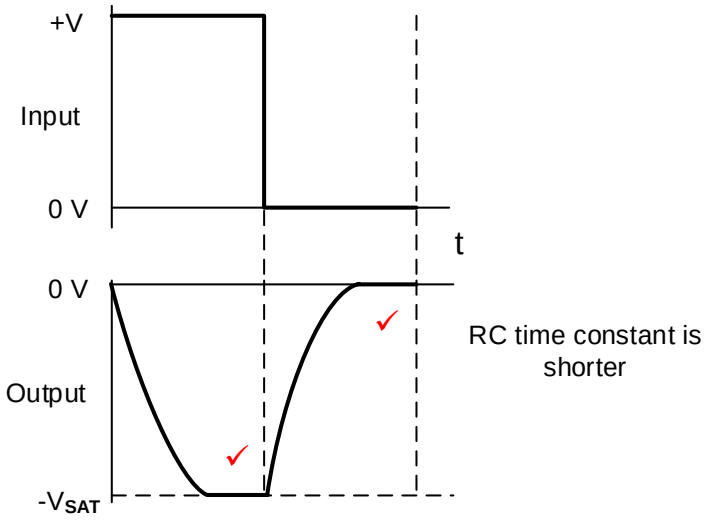
4.6.3 The Op-amp is used in open loop mode therefore; ✓ there is no feedback loop to limit the gain of the Op-amp, ✓ driving it into saturation. (2)

4.7
- When the square wave input rises, both plates of the capacitor initially rises to the voltage of the square wave input. ✓
- As the left hand plate is held high, while the right-hand plate discharges through resistor R. ✓
- When the square wave falls to zero, the capacitor cannot discharge instantly, ✓ so both its plates follow the input voltage, instantly falling, with the left plate at zero and the right plate forced down to a value more negative than its initial charge. ✓
- The right-hand plate then discharges, falling to zero. ✓ (5)

4.8 4.8.1

- On applying a square wave to the integrator input, the input voltage immediately rises to a steady positive value. ✓
- The input resistor then has a fixed voltage on the one end and a virtual ground 0 V at its other end. ✓
- According to Ohm's law, this will cause a fixed current to flow, ✓ which is fed via the virtual ground point to the capacitor, charging it at a rate of R x C = t. ✓
- As the Op-amp's inputs are both at 0 V, it holds the left-hand plate of the capacitor at 0 V, ✓causing the right-hand plate to steadily fall in voltage. ✓ In line with the discharging characteristics of a capacitor. (6)

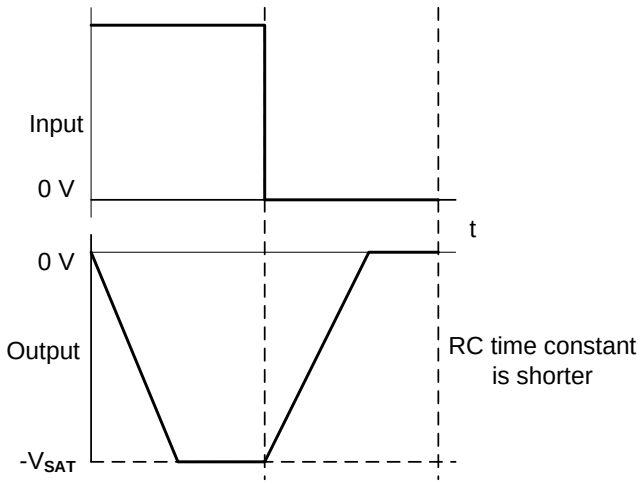
4.8.2



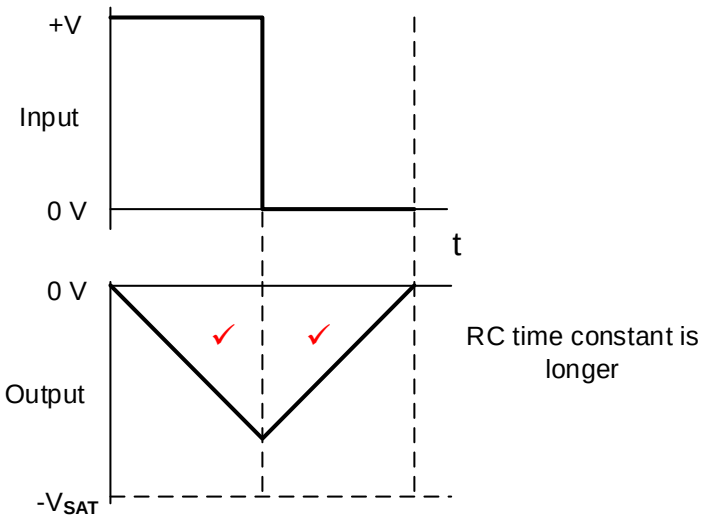
(2)

NOTE: 1 mark for inversion
1 mark tops and bottoms being clipped

Due to this being an active op-amp integrator, and not a passive circuit the following response will also be considered:



4.8.3



(2)
[60]

QUESTION 5: AMPLIFIERS

5.1 5.1.1 Feedback is defined as a process whereby a part of the output signal ✓ is fed back to the input stage.✓ (2)

5.1.2 Distortion is defined as a condition that will occur when the amplification is no longer linear ✓ in form or frequency. ✓ (2)

Distortion is an undesired change of a signal passing from the input to the output stage of an amplifier circuit.

NOTE: If frequency is not mentioned, but the learner demonstrates the understanding of additional factors causing distortion or the alteration of the wave shape, the second mark will be awarded.

5.2 5.2.1 RC coupled Amplifier. ✓
Common Emitter Amplifier. (1)

5.2.2 The emitter-base junction (EB) must be forward biased above the cut-off region ✓ and below the saturation region. ✓ The collector-base junction (CB) must be reversed biased ✓ for the transistor to operate in the Active region for amplification to take place.✓

OR

The values of resistors R_1 and R_2 must be chosen so that the Q point of the transistor is biased in the middle of the load line allowing for 360° of the input signal to be amplified. (4)

5.2.3 $V_{RC} = V_{CC} - V_{CE}$ ✓
$= 9 - 2{,}38$ ✓
$= 6{,}62\,V$ ✓ (3)

OR

$V_{CC} = V_{CE} + (I_C \times R_C)$
$9 = 2{,}38 + (I_C \times 470)$
$I_C = 14{,}09\,mA$

$V_{RC} = I_C \times R_C$
$V_{RC} = 14{,}09 \times 10^{-3} \times 470$
$V_{RC} = 6{,}62\,V$

For the alternative method marks will be awarded as follows:
1 mark for the first calculation
2 marks for the correct final calculation

NOTE: V_{RE} is included in the value of V_{CE} as shown in the data on the circuit diagram.
In the case of a learner indicating that he cannot calculate V_{RC} due to V_{RE} not being indicated separately on the diagram, 3 marks will be awarded.
In the case of no answer, 0 marks.

5.2.4 $A_V = 20\log\frac{V_{OUT}}{V_{IN}}$ ✓
$= 20\log\frac{2{,}38}{2\times10^{-3}}$ ✓
$= 61{,}51\,dB$ ✓ (3)

5.2.5 When V_{IN} increases then V_{BE} will increase above the Q point ✓ and T_1 is switched on harder. ✓ The internal resistance of T_1 is reduced due to an increased base current. ✓ I_C increase and V_{CE} reduces ✓ due to lower resistance of T_1 and increase in I_C. The result is reduction in output voltage and 180° phase shift. ✓ The gain of a transistor is fixed. (5)

5.3 A = Base current (I_B) ✓
B = Base-emitter voltage (V_{BE}) ✓
C = Input Voltage ✓ OR change in V_{BE} (ΔV_{BE}) (3)

5.4 5.4.1 Push-Pull Amplifier. ✓ (1)

5.4.2 NPN transistor. ✓ (1)

5.4.3 Each transistor is biased for Class B (180°) amplification ✓ when no signal is applied to the input transformer, no alternating signal is applied to the base of Q_1 and Q_2. ✓ Because the Q point is so low, no current will flow in the circuit. ✓ (3)

5.4.4
- The input transformer has a centre-tapped secondary which acts as a splitter to produce two equal ✓and opposite signals during each half-cycle. ✓
- Transistors Q_1 and Q_2 conduct when its base becomes positive with respect to its emitters ✓ each amplifying the alternate half input signal.
- The centre-tapped output transformer combines the two half-cycles to produce one complete cycle. ✓ (Class A result)
- Each transistor conducts for alternate half-cycles only. ✓ (Class B amplification) (5)

5.5 5.5.1 Class C amplification. ✓ (1)

5.5.2 Radio Frequency (RF) amplifiers are narrow band amplifiers ✓ capable of amplifying only the band of frequencies ✓ which is the information carrier and suppresses all other frequencies. ✓ (3)

5.5.3 The resonating frequency of the circuit can be varied by adjusting the value of the variable capacitors. ✓ (1)

5.5.4 Band pass filter. ✓ (1)

5.5.5 Energy transfer in the tank circuit is achieved when the tank circuit oscillates at the resonant frequency. ✓ When the amplifier receives an input signal which is amplified via T_1, this amplified audio signal is modulated onto the resonant radio frequency of the tank circuit. ✓ The result is a mixed output signal that includes the resonant radio frequency of the tank circuit as well as the modulated audio signal. ✓ (3)

5.6 5.6.1 Hartley Oscillator. ✓ (1)

5.6.2
- When first switched ON, the collector voltage rises and allows the capacitor in the tank circuit to charge. ✓
- The voltage drop across the inductors is in an inverted form, driving the transistor's base in the opposite direction thereby switching it OFF. ✓
- The capacitor will discharge through the inductors and push the tank circuit into oscillation. ✓
- During oscillation the voltages at each end of the tank circuit are 180° out of phase with each other, relative to their 0 V common centre tap point. ✓
- This ensures that the collector voltage is 180° out of phase with the base voltage. ✓
- The freewheeling effect of the tank circuit's operation then begins to drive the transistor alternately ON and OFF which in turn continually re-charges the tank circuit keeping it oscillating at a constant amplitude. ✓ (6)

5.6.3 Feedback in the circuit is obtained with the signal being fed back from the collector terminal of Q_1 ✓ through capacitor C_1 that is connected to the resonating tank circuit ✓ which are 180° out of phase with each other ✓ and then through capacitor C_2 to the base of transistor Q_1. Q_1 is in common emitter configuration which creates another 180° phase shift. ✓ (4)

5.6.4 Inductor L_3 is a RF choke used to prevent ✓ the AC resonant signal from being fed back to the base via R_1 at 180° phase shift through the DC supply ✓ which will cause the oscillations to fade away quickly. ✓ (3)

5.7 The FET will minimise the loading effect ✓ on preceding stages, as it has a higher input impedance when compared to the relatively low input impedance of the Bipolar Junction transistor (BJT). ✓ (2)

5.8
- They both produce a pure sinusoidal output waveform.✓
- They both use positive feedback. ✓
- They both use a tank circuit for oscillation.
- They both use a transistor for amplification.

(2)
[60]

TOTAL: 200