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Department: Basic Education **REPUBLIC OF SOUTH AFRICA**

ELECTRICAL TECHNOLOGY (ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS (PAT)

GRADE 12

2023

These guidelines consist of 49 pages.

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1.

INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- AGRICULTURE: Agricultural Management Practices, Agricultural Technology
 - ARTS: Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- SCIENCES: Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- SERVICES: Consumer Studies, Hospitality Studies, Tourism
- TECHNOLOGY: Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps needs to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for ELECTRONICS.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2023 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
 - Enclosure:
 - The file must include a design.
 - The enclosure and the design must match.
 - No cardboard boxes are allowed.
 - Plastic wooden and metal enclosures are acceptable.
 - Enclosures that are manufactured and/or assembled by the learners are preferred.
 - The enclosure should be accessible for scrutiny inside.
 - Lids that are secured are preferred.
 - Circuit board:
 - The file should include the PCB design.
 - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
 - Switches, potentiometers, connectors and other items must be mounted.
 - Wiring must be neat and bound/wrapped.
 - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
 - Logo and name:
 - The file should contain the logo and name design and specification plate.
 - Logo, specification plate and name must be prominent on the enclosure.
 - The logo/specification plate must be affixed in a permanent manner painted, glued or stuck on with vinyl.

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the FIRST THREE TERMS and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must NOT be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a working model and model answer file that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. No re-assessment will be done once the facet sheets have been completed and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2023	Teacher – Builds the models and works out the model answers for the simulations. Identifies shortages in tools, equipment and consumable items for simulations that must be procured. SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2023	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holidays
January 2023	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to
February 2023	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2023	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holidays
April–June 2023	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate Simulation 1 10% of learners' work is moderated
April–June 2023	PAT project – learners continue with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions every week for learners to complete the PAT project Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2023	PAT intervention	Learners that are behind on the PAT are required to complete the project during these holidays.
July–August 2023	Moderation of Simulation 2	District subject facilitator/subject specialist will visit the school and moderate Simulation 2 – different learners from the previous term 10% of learners' work is moderated
July–August 2023	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed
September– October 2023	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly

2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulation 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT, the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. All four simulations will be moderated.
- The teacher is required to build an exemplar model of each project type chosen for the school.
- This model must be on display during moderation.
- The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).
- Level 5 assessments must exceed the model of the teacher in skill and finishing.
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.
- The moderator will randomly select no fewer than two projects (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit the outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who make use of simulation programs on a computer may use them for the learners to practise on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

- STEP 1: The teacher will choose simulations from simulations that are provided.
- STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items get lost/damaged very easily when learners work on them.
- STEP 3: Contact three different electronics component suppliers for comparative quotations.
- STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
- STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
- STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/resource availability.

Teachers are required to develop a set of model answers in the teacher's file. Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided by schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects vary in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They MUST redraw these circuits in their files correctly.

The description of the operation of the circuits is NOT complete. Learners are required to interrogate the function of the components in the provided circuit. Learners should elaborate on the purpose of components in the circuit. It is recommended that learners investigate similar circuits available on the internet and in the school library or workshop reference books.

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2.8

Working mark sheet (A working Excel file is provided with this PAT.)

ΡΑΤ	mark sheet	Term 1	Term 2	Pro	oject	Total = Term 1 +	00	ark
		Simulation 1	Simulation 2	Design and Make Part 1	Part 2	Term 2 + Project	Mark out of 100	Moderated Mark
No.	Name of Learner	50	50	120	30	250	Σ	Š
1.								
2. 3.								
3. 4.								
4. 5.								
6.								
7.								
8.								
9.								
10.								
11.								
12.								
13.								
14.								
15.	T - (- 1							
	Total							
	Average							
Teach	er Name:	Principal Name:		Mode	erator Name:			
Signat	ure:	Signature:		Signa	ature:			
Date:		Date:		Date	:			

3. LEARNER GUIDELINES

3.1 PAT 2023 COVER PAGE

(Place this page at the front of the PAT.)

Time allowed: Terms 1–3	(2023)
Learner Name:	
Class:	
School:	
Specialisation: EL	ECTRONICS
Complete any TWO simu	lations.
Project (Write the name of	of the project):
vidence of moderation:	

When the learner evidence selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
District moderation				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation 1	50		
Simulation 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
Total	250		

3.2 Instructions to the learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work and co-operative work are NOT allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain TWO simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO decimals. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and may be in colour or greyscale. Scanned photos and photocopies are allowed.
- This document must be placed inside your PAT file together with the other evidence.
- Learners with identical photos will be penalised and receive zero for that section.

3.3 Declaration of Authenticity (COMPULSORY)

Declaration:

I ______ (name) herewith declare that the work represented in this evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

Signature of learner

Date

4. SIMULATIONS

4.1 Simulation 1: RLC series circuit

Name of learner:				
Class:	Date Completed:	Mark	50	
Date Assessed:	Assessor Signa	ature:		
Date Moderated:	Moderator Sign	ature:		

4.1.1 **Purpose:**

- To build an RLC series circuit
- To observe the effect of the change in frequency from resonance on RLC series • circuit
- To compare the measured and the calculated values

4.1.2 **Procedure:**

Build the series RLC circuit in FIGURE 4.1.4 on the breadboard using the components provided.

Connect the circuit to a function generator.

Set the output signal voltage of the function generator to 5 V with a frequency of 50 Hz.

Take the measurements as asked in TABLE 4.1.5 with the frequency adjusted to 50 Hz, 159 Hz and 500 Hz and then answer the questions that follow.

4.1.3 **Required resources:**

COMPONENTS	TOOLS AND EQUIPMENT	
$R_1 = 100 \Omega$ resistor	Multimeter	
$L_1 = 10 \text{ mH}$ inductor	Function generator	
$C_1 = 10 \ \mu F$ capacitor	Leads	
	Breadboard	
	Side cutters	
	Pair of pliers	
	Oscilloscope	

4.1.4 **Circuit diagram:**

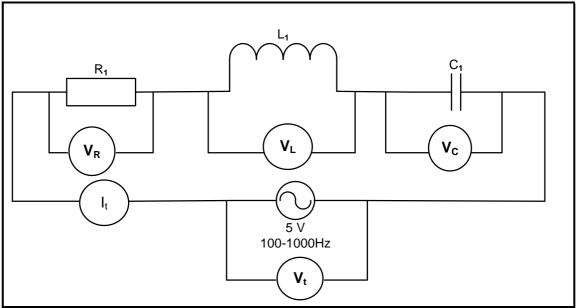


FIGURE 4.1.4: RLC CIRCUIT DIAGRAM

4.1.5 Complete TABLE 4.1.5 by entering measured values of V_{R} , V_{L} , V_{C} , V_{T} and I_{T} .

NOTE: Alternatively measure with the oscilloscope and convert to V_{ms} values.

METERS CONNECTED ACROSS	MEASUREMENTS AT 503 Hz	MEASUREMENTS AT 100 Hz	MEASUREMENTS AT 1 000 Hz
V _R			
VL			
Vc			
V _T			
I _T			



- 4.1.6 Study the measurements in TABLE 4.1.5 above and answer the following
 - (a) Compare the values of V_L and V_c at 503 Hz.

(2)

(13)

$X_L = 2\pi f L$	$X_C = \frac{1}{2\pi fC}$			
X _L =	$X_c =$			
Compare the values of V_L and V_L	/ _c at 1 000 Hz.			
Calculate the values of X_L and λ	X ₂ at 1 000 Hz			
$X_L = 2\pi f L$				
$\Lambda_L = 2\pi J L$	$X_C = \frac{1}{2\pi f C}$			
X _L =	Xc =			
Compare the values of V _L and V _c at 503 Hz.				
Calculate the values of X_L and λ	X _c at 503 Hz.			
$X_L = 2\pi f L$	$X_C = \frac{1}{2\pi fC}$			
X _L =	X _c =			

Theory Simulation 1: (4) (35)

4.1.7

NOTE: Learner competency in this context will mean the following: (This is done for easy assessment when using a rubric.)

Not yet	Have not met the requirements and will be given another opportunity for re-						
competent	assessment.						
	• Be precise about what they did wrong, or the areas they need to improve in.						
	• Explain clearly the level of skill they need to achieve to be assessed as 'competent'.						
	Indicate whether part or all of the assessment event will need to be repeated.						
Competent	Have the necessary ability, knowledge or skill to complete the task successfully.						
	Acceptable and satisfactory, though not outstanding.						
Outstanding	Went beyond expectation (neatness, proficiency – high degree of skills, expertise)						

FACET SHEET FOR SIMULATION 1

	Mark al	location (tick the appropriate I	evel next to the task indica	ted)	
Task description	Competent after reassessment of certain/all parts of the task	Not yet competent after reassessment of certain/ all parts of the task	Competent	Outstanding (Highly competent)	Allocation of marks
Building the RLC Circuit	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.	The learner correctly built the circuit without the guidance of the teacher.	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency.	9
	(1–2)	(3–4)	(5–6)	(7–9)	
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments.	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments.	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being		
	(1)	(2)	reminded by the teacher.		3
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded.	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.		3
	(0)	(1–2)	(3)		0
Rubric Theory Total Simulation 1					/15 + /35 = /50

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4.2 Simulation 2: Inverting op amp

Name of learner:		_		
Class:	Date completed:	Mark	50	
Date Assessed:	Assessor Sig	nature:		
Date Moderated:	Moderator Sig	gnature:		_

4.2.1 **Purpose:**

- To build an inverting operational amplifier circuit using a 741 op-amp integrated circuit (IC)
- To display the output waveforms on an oscilloscope
- To observe how a change in the value of R_F affects the gain and output voltage of the circuit

4.2.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Analogue/Digital oscilloscope (dual trace) Function generator Multimeter Variable DC power supply (split supply) Side cutters Wire strippers Long-nose pliers Breadboard	1 x LM 741 op-amp 2 x 10 kΩ for R _{IN} and R _F 1 x 15 kΩ, 22 kΩ, 33 kΩ, 47 kΩ, 56 kΩ and 82 kΩ for R _F Connecting wires

4.2.3 **Procedure:**

Construct the circuit in FIGURE 4.2.3 on a breadboard.

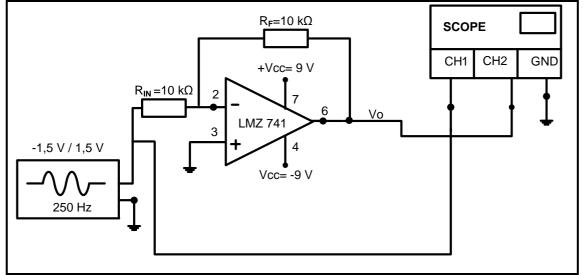
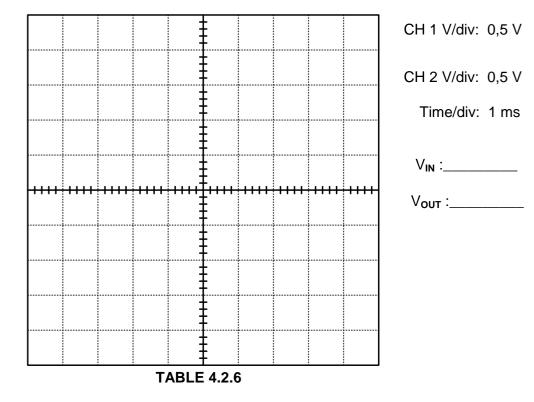


FIGURE 4.2.3: INVERTING OP-AMP

- 4.2.4 Ensure CH1 and CH2 are set to 0,5 V /division. The time setting must be set on 1 ms/division..
- 4.2.5 Draw and label both the input (from CH1) and output (from CH2) waveforms for TWO complete cycles on the table below.
- 4.2.6 Write down the peak values of the input and output voltage readings from CH1 and CH2 with R_F = 10 k Ω .



NOTE: 2 marks for each correct waveform

4.2.7 Use the peak values in QUESTION 4.2.6 to calculate the gain below. (ALL values measured with the oscilloscope are peak values.)

$$A_{V} = -\left(\frac{V_{OUT(peak)}}{V_{IN(peak)}}\right)$$

$$= \underline{\qquad}$$

$$= \underline{\qquad} \qquad (2)$$

4.2.8 Calculate the voltage gain of the circuit by using the formula below.



4.2.9 Measure and record the voltages across V_{OUT} in the table below. Also calculate the voltage gain values in the table below as you change the value of R_F in the circuit.

Use
$$A_V = -\left(\frac{V_{OUT}}{V_{IN}}\right)$$

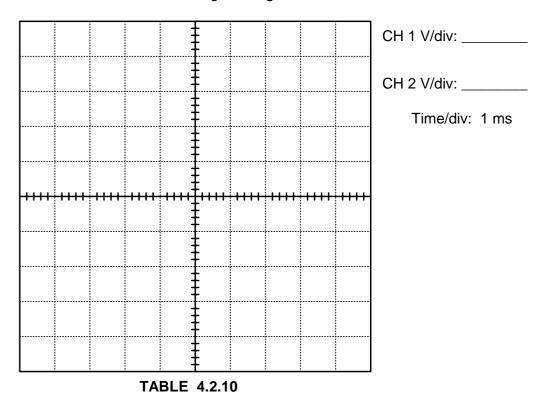
RESISTOR R _F	V _{IN}	V _{out}	VOLTAGE GAIN (A _v)
(a) 22 kΩ	1,5 V		
(c) 47 kΩ	1,5 V		
(d) 100 kΩ	1,5 V		

TABLE 4.2.9

NOTE: 1 mark for each correct voltage value = 3 2 marks for each correct gain calculation = 6

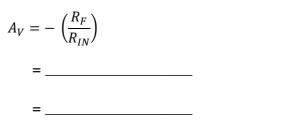
(9)

4.2.10 Draw and label the input and output waveforms for at least two complete cycles in the table below. Indicate the voltage settings for CH 1 and CH 2 with $R_F = 100 \text{ k}\Omega$.



NOTE: 2 marks for each correct waveform 1 mark for each voltage setting

4.2.11 Calculate the gain of the amplifier by using resistance values when $R_F = 100 \text{ k}\Omega$.



4.2.12 Refer to TABLE 4.2.9, your waveforms in TABLES 4.2.6 and 4.2.10 as well as your calculations in 4.2.8 and 4.2.11. Compare the gain in TABLE 4.2.8 to the gain in QUESTION 4.2.11 above and write a conclusion to your findings.

(5)

(6)

(2)

Theory Simulation 2: (32)

NSC

FACET SHEET FOR SIMULATION 2

	Mark al	location (tick the appropriate I	evel next to the task indica	ted)	
Task description	Not yet competent after reassessment of certain/all parts of the task	Competent after reassessment of certain/ all parts of the task	Competent	Outstanding (Highly competent)	Allocation of marks
Building the inverting op- amp using LM 741 IC	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.	The learner correctly built the circuit without the guidance of the teacher.	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency.	12
-	(1–3)	(4–6)	(7–9)	(10–12)	
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments.	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments.	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being		
	(1)	(2)	reminded by the teacher. (3)		3
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded. (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (3)		3
				Rubric Theory Total Simulation 2	/18 + /32 = /50

4.3 Simulation 3: Switching circuits using a 555 IC and a 741 op amp

Name of learner:				
Class:	Date Completed:	Mark	50	
Date Assessed:	Assessor Signatur	e:		
Date Moderated:	Moderator Signatu	ire:		

4.3.1 **Purpose:**

- To build an electronic piano (astable multivibrator) circuit using a 555 IC on a breadboard as shown in FIGURE 4.3.3
- To display the output waveforms on an oscilloscope
- To calculate the output frequency
- To investigate how a change in R_{IN} affects the frequency and tone of the output

4.3.2 **Resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	1 x 555 timer IC
Analogue/Digital oscilloscope	1 x 100 nF capacitor
Variable DC power supply	1 x 10 µF (electrolytic capacitor 25 V)
Side cutters	$5 \times 1 \text{ k}\Omega$ resistor
Wire stripper	1 x 10 k Ω potentiometer
Long-nose plier	1 x 8 Ω speaker/buzzer
Breadboard	5 x push buttons
	Connecting wires

4.3.3 Procedure:

- (a) Build the circuit in FIGURE 4.3.3 on the breadboard.
 - Set the 10 k Ω POT to 6,5 k Ω before connecting it in the circuit.
 - Connect channel 1 of the oscilloscope to pin 3 of the 555 IC.
 - Switch the circuit ON, press the push buttons (one at a time) and observe.
 - Answer the questions that follow.

NOTE: If there is noise, pin 5 can be connected to ground via a capacitor of $(0,01 \ \mu\text{F})$

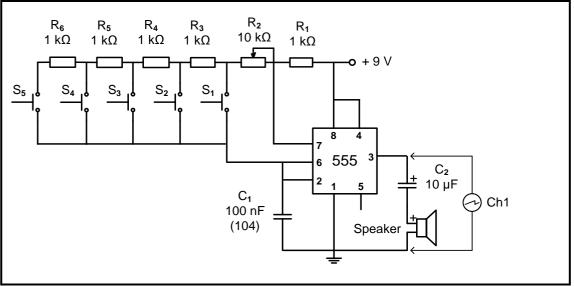
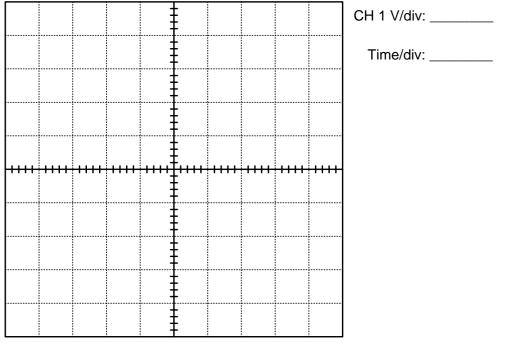
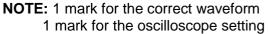


FIGURE 4.3.3: ASTABLE MULTIVIBRATOR

(b) Press push button S₁ and draw the output wave observed on the oscilloscope grid provided. Set the oscilloscope to display at least FOUR complete cycles.





(2)

(c) Make use of the oscilloscope settings and determine the frequency of the signal.

Frequency when S_1 is pressed.

(2)

(d) Press push button S_5 and draw the output wave observed on the oscilloscope grid provided. Do NOT adjust the time per division setting.

						Time/div:
 	-	E I			 	
		-				
 	-				 	
 ++++	++++			++++	 	
 	-				 	
 	-				 	
 	-	-			 	
	-					
			mark for the correct wa			

1 mark for the oscilloscope settings

(e) Make use of the oscilloscope settings and determine the frequency of the signal.

Frequency when S_5 is pressed.

- Press each of the push buttons and observe.
 Explain why there is a difference in the output for each push button.
 - (2)Theory Simulation 3A:(10)

(2)

(2)

FACET SHEET FOR SIMULATION 3A

	Mark a	allocation (tick the appropri	ate level next to the task indic	ated)	
Task description	Competent after reassessment of certain/all parts of the task	Not yet competent after reassessment of certain/ all parts of the task	Competent	Outstanding (Highly competent)	Allocation of marks
Building the astable multivibrator using 555 IC	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.	The learner correctly built the circuit without the guidance of the teacher.	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency.	9
	(1–2)	(3–4)	(5–6)	(7–9)	
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		3
Attitude/	The learner was reluctant to	The learner was reluctant	The learner demonstrated		
Behaviour/ Conduct	work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even	to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation	willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.		
	after being cautioned/ reprimanded.	and workshop practice.			3
	(0)	(1–2)	(3)		
				Rubric Theory	/15 + /10
				Total Simulation 3A	= /25

Simulation 3 B: Schmitt trigger using 741 IC

4.3.4 **Purpose:**

- To build the Schmitt trigger circuit in FIGURE 4.3.6 using a 741 op amp and display the input and output waveforms on an oscilloscope
- To investigate the effect of the R_{F} to R_1 ratio on the trigger voltage and output of the circuit

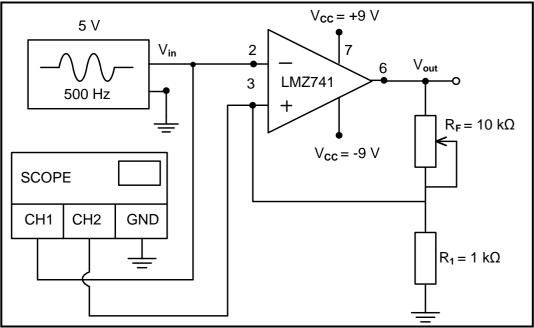
4.3.5 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Function generator Dual trace oscilloscope +9 V 0 V -9 V DC power supply Side cutters Wire stripper Calculator	1 x LM741 op amp 1 X 1 kΩ resistor 1 x 10 kΩ potentiometer Connecting wires

4.3.6 **Procedure:**

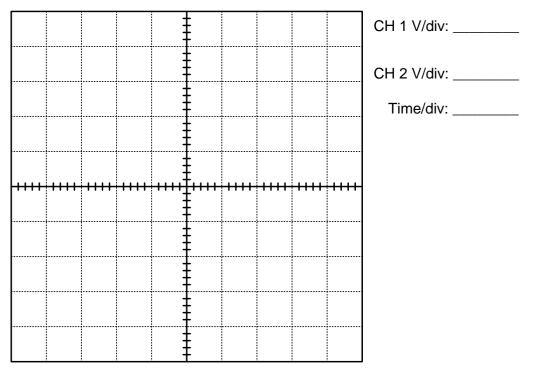
- Set the dual voltage power supply to +9 V / -9 V.
- Set the function generator to deliver 5 V peak 500 Hz sine wave.
- Build the circuit in FIGURE 4.3.6(a) on your experiment board and connect it to the supply and input.
- Connect channel 1 of the oscilloscope across the inverting input to display at least TWO complete cycles.
- Connect channel 2 of the oscilloscope across the non-inverting input to display at least TWO complete cycles.
- Ensure that the V/div settings for channel 1 and channel 2 are the same.
- Set the T/div setting to display at least TWO complete cycles of the input and output.
- After measuring the voltage on the non-inverting input, use channel 2 to display the output.

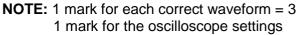
(a) Build the circuit in FIGURE 4.3.6(a) on the experiment board.



- FIGURE 4.3.6(a): 741 SCHMITT TRIGGER
- (b) Draw and label the input waveforms from pin 2 and pin 3 on the oscilloscope grid below.

Keeping the V/div settings the same, change channel 2 connection from pin 3 to pin 6 (output) and draw and label the output waveform on the oscilloscope grid below.





(c) Set R_F resistor to the following values and complete TABLE 4.3.6 (c) below.

R _F	NON-INVERTING VOLTAGE (PIN3)
8 kΩ	
5 kΩ	
2 kΩ	

TABLE 4.3.6(c)

(d) Refer to TABLE 4.3.6(c) above and give your observation when changing the value of R_F . Write a conclusion about the effect of the R_F to R_1 ration on the trigger voltage levels of the Schmitt trigger.

(3)

(3)

- Theory 3B: (10)
- Activity 3B: (15)
- Total Simulation 3: [50]

FACET SHEET FOR SIMULATION 3

	Mark	allocation (tick the appropriate	e level next to the task indicated	ated)	
Task description	Competent after re- assessment of certain/all parts of the task	Not yet competent after re- assessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	Allocation of marks
Building the Astable multivibrator using 555 IC	The learner was given opportunities to re-build the circuit after the teacher intervened in identifying and rectifying more mistakes (1–2)	The learner was given an opportunity to re-build part of the circuit after the teacher intervened in identifying and rectifying few mistakes (3–4)	The learner correctly build the circuit without the guidance of the teacher (5–6)	The learner correctly build the circuit without the guidance of the teacher and went beyond expectations and with high proficiency (7–9)	9
Safety aspects	The learner was timeously reminded to apply safety rules, regulation, and correct procedure when using tools and instruments (1)	The learner was sometimes reminded to apply safety rules, regulation, and correct procedure when using tools and instruments (2)	The learners applied safety rules, regulation, and correct procedure when using tools and instruments to wire the circuits without been reminded by the teacher. (3)		3
Attitude/ Behaviour/ Conduct	The learner was reluctant at all to work, cooperate, take responsibility of their own conduct, and follow instructional, regulation and workshop practice even after been cautioned/reprimanded (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct, and follow instructional, regulation and workshop practice (1–2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct, and follow instructions, regulation and workshop practice. (3)		3
				Rubric Theory Total Simulation 3B Total Simulation 3A TOTAL:	/15 + /10 = /25 + /25 = /50

4.4 Simulation 4: Push-pull amplifier

Name of learner:				
Class:	Date completed:	Mark	50	
Date Assessed:	Assessor Signat	ure:		
Date Moderated:	Moderator Signa	ature:		

Activity 4.4: Push-pull amplifier

4.4.1 Purpose:

- To build a push-pull amplifier circuit using discrete components ٠
- To measure/calculate voltages and gain of the circuit •

4.4.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue /Digital trainer	2 x 4k 7 Ω resistors for R ₁ and R ₂
Analogue/Digital oscilloscope	2 x 10 Ω resistors/ 1 W resistors for R ₃ and R ₄
Function generator	1 x 1 k Ω resistor for R _L
Multimeter	1 x 22 μ f capacitor for C ₁
Variable DC power supply	1 x 10 μ f capacitor for C ₂
Side cutters	1 x BFY transistor for Q ₁
Wire stripper	1 x 2N2905A for transistor Q ₂
	2 x 2N4007 diodes for D_1 and D_2

4.4.3 **Procedure:**

Build the circuit in FIGURE 4.4.3 on the breadboard. The signal generator must be set on 0,5 V peak to peak with a frequency of 5 kHz.

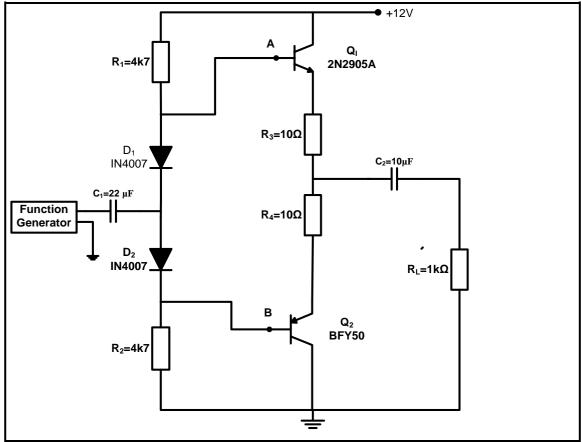
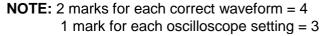


FIGURE 4.4.3: PUSH-PULL AMPLIFIER

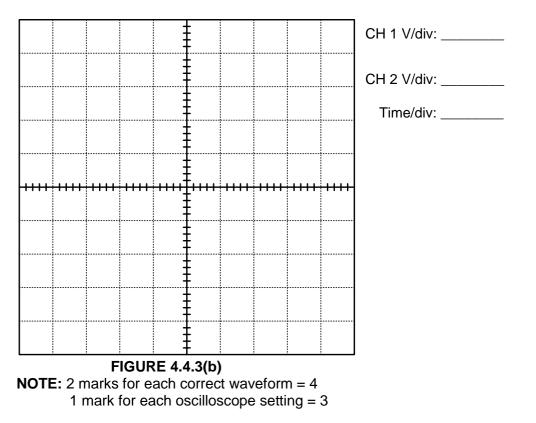
(a) Connect CH1 of the oscilloscope to point (A) and CH2 to point (B) and display the waveforms. Draw the waveforms for at least TWO complete cycles on the oscilloscope grid in FIGURE 4.4.3(a).

				-	-					CH 1 V/div:
				-	-					CH 2 V/div:
				-						
				-	-					Time/div:
				-	Ē					
				-	-					
+++++	••••	••••	••••	+++++	<u></u>	++++	++++	++++	++++	
				-	Ē					
				-	-					
				-	-					
				-	<u> </u>					
				-	È					
				-	-					
			FIC		1 1 3	(a)				-

FIGURE 4.4.3(a)



(b) Connect CH1 of the oscilloscope to the function generator and CH2 across the load resistor R_{L} to display the input and output waveforms. Draw the input and output waveforms for at least TWO complete cycles in FIGURE 4.4.3(b).



(7)

(7)

(C) Write down the function of D1 and D2.

(d) Identify the class in which the transistors are biased. Motivate your answer.

(3)

(4)

(2)

(2)

Complete the table below. (e)

	V _{p-p}	V _{rms}
Input waveform		
Output waveform		

(f) Calculate the base voltage with the following formula: $V_b = \frac{R_2}{R_1 + R_2} \times \frac{V_{cc}}{1}$

(g) Calculate the power gain in dB using the following formula: D

$$A_P = 10\log\frac{P_{out}}{P_{in}}$$

(2)

(h) Calculate the voltage gain using the following formula: $A_V = 20 \log \frac{V_{out}}{V_{in}}$

Write a conclusion about the wave shape of the input and output waveforms. (i) Motivate your answer.

- (j) Write a conclusion about phase sequence of the input and output waveforms. Motivate your answer.
- (3)

(3)

(2)

Theory 4: (35)

34

FACET SHEET FOR SIMULATION 4

	Mark allocation (tick the appropriate level next to the task indicated)						
Task description	Competent after reassessment of certain/all parts of the task	Not yet competent after reassessment of certain/ all parts of the task	Competent	Outstanding (Highly competent)	Allocation of marks		
Building the astable push pull amplifier	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. (1)	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. (3–4)	The learner correctly built the circuit without the guidance of the teacher. (5–6)	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. (7–9)	9		
Safety aspects	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		3		
Attitude/ Behaviour/ Conduct	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded. (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (1–2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (3)		3		
				Rubric Theory TOTAL SIMULATION 4	/15 + /35 = /50		

5. **SECTION B: DESIGN AND MAKE**

Design and Make Project		
Time: January to August 2023		
Learner Name:		RECEIPTION OF
School:		
Class:		
Title/Type of Project:		

INSTRUCTIONS

- This section is COMPULSORY for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to): .
 - Seven components 0
 - A variety of components (both active and passive) 0
 - PCB making in some form 0
 - Soldering 0
 - An enclosure with a switch and protection 0
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST

The learner MUST fill in this checklist BEFORE marking of the section takes place.

NO.	DESCRIPTION	TIC	(⊠)		
		NO	YES		
Design	and Make: Part 1				
1.	Circuit diagram drawn				
2.	Circuit description filled in				
3.	Component list completed				
4.	Tools list for circuitry populated				
5.	Measuring instrument list filled in				
Design	and Make: Part 2				
1.	Enclosure design completed and included in the file				
2.	Unique name written down and on the enclosure				
3.	Logo designed and on the enclosure				
Miscell	Miscellaneous				
1.	Enclosure included in the project				
2.	Enclosure prepared and drilled according to the design				
3.	Enclosure finished off and completed with name and logo				
4.	PCB securely mounted in the enclosure using acceptable techniques				
5.	Circuit inside the enclosure accessible				
6.	Internal wiring neat and ready for inspection				
7.	File and project completed and ready for moderation at the workshop/room				

5.1 Design and Make: Part 1

5.1.1 **Circuit diagram**

Draw a circuit diagram of the project chosen and paste it on the next page.

5.1.2 **Project: Description of operation**

Use the space below to describe how the project operates. Do research and use your own words.



DBE/PAT 2023

5.1.3 **Component list**

List the components you will need for the circuit diagram.

LABEL	DESCRIPTION AND VALUE	QUANTITY
L	1	

5.1.4 **Tools/Instrument list**

List the tools needed to complete the project.

DESCRIPTION	PURPOSE

5.2 Assessment of the Design and Make Phase: Part 1

NO.	FACET DESCRIPTION	Mark	Achieved mark
Circu	it Diagram	•	-
1.	The circuit diagram was drawn using	6	
	EGD equipment (4)		
	CAD/Any electronic design software (6)		
2.	The circuit diagram was drawn using correct symbols.	3	
3.	The circuit diagram has all labels, e.g. R1, C1, Tr1	3	
4.	The circuit diagram has all component values, e.g. 100 $\Omega,$ 220 μF	4	
5.	The circuit diagram has a name/title.	2	
6.	The circuit diagram has a frame and title block.	2	
	Circuit Diagram Subtotal:	20	
Com	ponent List		
7.	Labels correlate with circuit diagram.	2	
8.	Description and values correlate with circuit diagram.	2	
9.	Quantities are correct.	1	
	Component List Subtotal:	5	
	Component List oubtotal.	5	
Desc	ription of Operation	I	
10.	Basic function of the circuit is described correctly. The purpose/role/function of each component is described.	11	
11.	All subcircuits in the circuit diagram and component list are included in the description.	4	
12.	Purposes of subcircuits in the circuit diagram are described correctly.	5	
13.	Learner used own interpretation and did not copy from another source verbatim.	3	
14.	Sources are acknowledged.	2	
	Description of Operation Subtotal:	25	
	S/Instrument List	4	
15.	The tools/instrument list has been completed.	4	
16.	The tools/instruments listed all have a purpose for being used.	1	
	Tools/Instrument List Subtotal:	5	

N	S	(
N	J	•	

NO.	FACET DESCRIPTION	Mark	Achieved mark
Circu	it Board Manufacturing		
17.	Transfer of the PCB design onto the blank board is correct. Not over-exposed or under-exposed.	5	
18.	Circuit board is etched neatly according to the PCB design.	10	
19.	The learner's name is etched onto the circuit design.	4	
20.	All burrs are removed.	2	
21.	Axial and radial components are placed neatly and flush with the board.	5	
22.	Component orientation is aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2	
23.	Soldered components – leads are cut off, flush and neat on the solder side.	5	
24.	More than 60% of the solder joints are shiny (not dry joints).	5	
25.	Wire insulation is stripped to the correct length (no extra copper showing).	3	
26.	Wiring is long enough to allow for dismantling and inspection.	2	
27.	Wiring is wrapped neatly.	2	
28.	A power switch is included and fitted to the enclosure.	2	
29.	A fuse/protection is included and fitted correctly where applicable.	2	
30.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2	
31.	Batteries/Transformer is mounted using a battery housing/ mounting bracket and battery clip (NO double-sided tape).	2	
32.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. LED is mounted with a grommet or applicable fitting. (Switch is on – must go out when fuse is blown.)	2	
33.	The project is fully operational and commissioned/installed in the enclosure.	10	
	Circuit Board Manufacturing Subtotal:	65	
	Circuit Diagram Subtotal:	20	
	Component List Subtotal:	5	
	Description of Operation Subtotal:	25	
	Tools/Instrument List Subtotal:	5	
	Circuit Board Manufacturing Subtotal:	65	

				TOTAL			
		(P/	ART 1 = 120) marks)			
NOTE:	In projects where facets are not appli	cable, t	he projects	should	be marked	and	the
	totals adjusted accordingly.						

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5.3 Design and Make: Part 2

5.3.1 Enclosure design

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.
- 5.3.2 Manufacture the enclosure neatly according to your design.
 You may use pre-cut panels from metal, wood and/or Perspex/Plexiglas. You must, however, construct/assemble these parts.
 Injection-moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.
- 5.3.3 Choose a name for your device. Write down the name of the device below.
- 5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.

5.4 Assessment of the Design and Make Phase: Part 2

NO.	FACET DESCRIPTION	Mark	Achieved mark
Enclos	sure Design		
1.	Enclosure design is included in first-angle orthographic projection.	2	
2.	Drawn design includes a title box and page border.	1	
3.	Isometric drawing included additionally.	2	
4.	Dimensions are included.	2	
5.	The name of the device is written in the PAT document.	1	
6.	The logo design and specification plate design is in the	2	
	PAT document.		
	Enclosure Design Subtotal:	10	
		10	
Enclo	sure Manufacturing		
7.	Enclosure matches the design.	1	
	Dimensions and placement correlate.		
8.	Name of the device is attached on the enclosure.	1	
9.	The logo design is attached on the enclosure.	2	
10.	The logo design on the enclosure is durable and not merely a	2	
	paper pasted on the enclosure (painted/used decoupage/screen		
	printed/sublimation printed).		
11.	The enclosure is manufactured from scratch/pre-cut parts.	5	
	Does NOT include: cardboard, paper, margarine container		
	Does include: sheet metal, Perspex, Plexiglas, wood, glass and		
	other raw materials, injection-moulded plastic boxes		
12.	Holes/Cut-outs in the enclosure are made with the appropriate	3	
10	tools.		
13.	Specification plate with the learner's name, operating voltage,	2	
	fuse rating and additional information on the project.		
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2	
15.	The circuit board is mounted using appropriate methods inside the	2	
	enclosure. (NO double-sided tape, Prestik, glue, chewing gum,		
	masking tape, etc.)		
	Fuele sure Menufestering Oak (state	20	
	Enclosure Manufacturing Subtotal:	20	

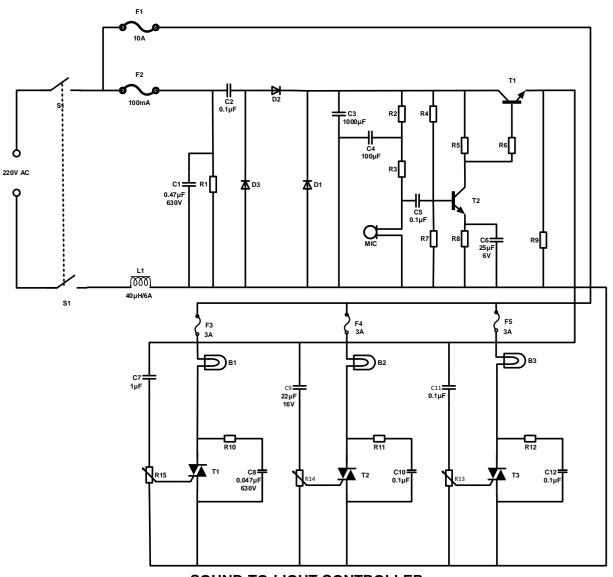
TOTAL	
(PART 2 = 30 marks)	

6.1 Practical Project 6.1: Sound-to-light Controller

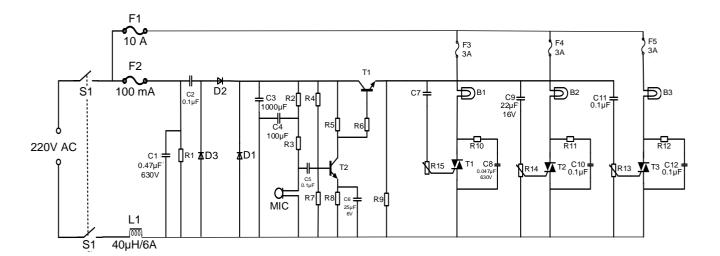
This sound-controlled lights circuit design is used to control the brightness of the lights attached to it in sync with the sound that is being captured by its microphone. This electronic circuit design is very common in disco houses, bars, parties, etc.

Usually, sound-controlled lights are just connected in parallel with the loudspeakers. This configuration has two disadvantages: first, a very powerful amplifier can destroy the lights, or worse, a defective light can destroy the amp. This problem is avoided by the circuit by not connecting directly to the amp. Instead, it picks up the sound with its microphone.

The power-supply part is on the left of the electret microphone amplifier and the light controller part is on the right. The capacitors C2 and C3 are the capacitive voltage dividers and reduce the power supply level. Diodes D1 and D2 rectify the positive swing of the AC voltage. The network, composed of L1 and C1, protects the power line from voltage surges. In this circuit design, an electret microphone is being used. Take note that there are two types of electret mics. The first type has three pins for power, ground and output. The second type has only two pins. The second type is used for this circuit.



SOUND-TO-LIGHT CONTROLLER



ALTERNATIVE CIRCUIT

NSC	

45

COMPONENT LIST			
R1 = 560 kΩ/1 W	C8, C12 = 0,047 µF/630V		
R2, R3 = 15 kΩ ¼ W	C9 = 22 µF 16 V		
$R4 = 33 k\Omega / \frac{1}{4} W$	C11 = 47 µF 16 V		
R5, R6, R9 = 1 kΩ ¼ W	D1, D2 = 1N4004		
R7 = 18 kΩ ¼ W	D3 = 1N4742 12v/1 W		
R8 = 560 Ω ¼ W	F1 10 A fuse 220 V		
R10, R11, R12 = 100 kΩ	F2 100 mA fuse 220 V		
P1, P2, P3 = 5 kΩ Pot	F3, F4, F5 220 V 3 A fuse		
C1 = 0,47 uF 630 V	L1 = 40 µH 6 A		
C2, C5 0,1 µF/220 V	B1, B2, B3 = 60 W incandescent lamp		
C3 1 000 µF/16 V	Mic = low-impedance microphone		
C4 100 μF/16 V			
C6 25 µF/6 V			
C7 1 µF 16 V			

WARNING:

Some parts in the circuit board are subject to lethal potential because the device is connected to 230 V AC. When plugging in the project, place it in a plastic or wooden box to prevent the circuit from shocking you. Avoid connecting this circuit to other appliances (e.g. to the output of an amplifier by means of a cable) because of the absence of a mains transformer. Use only the microphone in the main case to pick up the sound.

6.2 Practical Project 6.2: Dual voltage power supply

This project uses a centre-tapped transformer. The recommended rating of the transformer is 240 V to 18-0-18 V transformer.

NOTE: Sometimes the transformer you purchase outputs more than the specified value, so be careful when choosing the transformer.

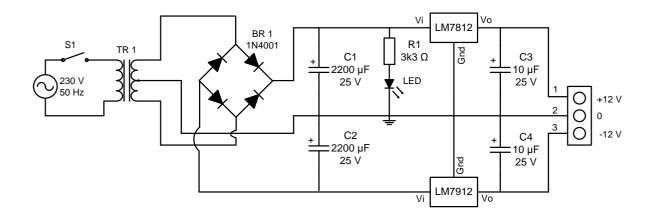
Capacitors C1 and C2 act as the smoothing capacitor; this is to even out any fluctuation in voltage. You can also add a bypass capacitor after the C1 and C2 to remove any AC noise which is not shown in the circuit. Besides the two voltage regulators, the 7812 gives positive 12 V and the 7912 gives negative 12 V. Other variants of voltage regulator ICs can also be used.

NOTE: 78xx gives the positive output & 79xx gives the negative output Capacitors C3 and C4 are used as the bypass capacitor to remove the AC noise and give a pure and cleaner DC Signal.

Required resources:

TOOLS	MATERIALS	
Multimeter Side cutters Wire strippers Soldering iron Helping hands PCB etching tank or	1 x transformer 240 to 15-0-15 volt - 4 x 1n4001 2 x 2 200 uF/25v 2 x 10 uF/25v 1 x 3,3 kΩ 1 x red LED	1 x 7812 voltage regulator IC 1 x 7912 voltage regulator IC 1 x toggle switch 1 x in-line fuse and holder 1 m mains supply cable 1 x 3 pin plug
similar Solder sucker	2 x heat sink 2 x 3 pin terminal block	1 x PCB

Circuit diagram:



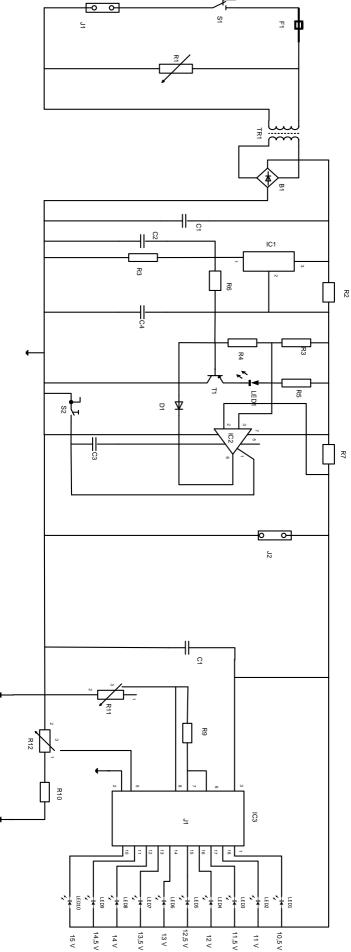
6.3 Practical Project 6.3: Automatic battery charger with battery-voltage bar-graph display

This automatic battery charger project is based on the National Semiconductor LM350 3 A adjustable regulator. It is designed to charge 12 V lead-acid batteries. When the switch SW1 is pushed, the output of the charger will go up to 14,5 V. The initial charging current is limited to 2 A. As the charge of the battery continues to rise, the charging current decreases to 150 mA and the output voltage is reduced to 12,5 V. At this stage the charging is terminated and the light-emitting diode lights up to indicate that the charging process has been completed.

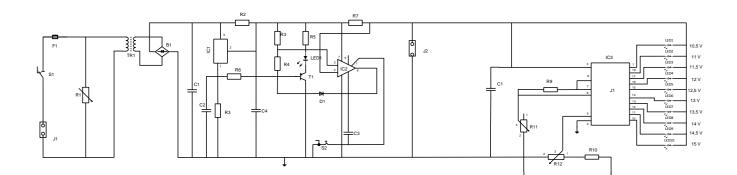
The schematic diagram below shows how the various components are connected. The first part of the diagram shows how the DC power supply to LM350 is achieved. The combined use of varistor V1 and fuse F1 is to protect the circuit from overcurrent and power surge of the mains supply.

Transformer T1 is used to step down the input voltage from the mains to 16 V AC. Diode bridge DB and electrolytic capacitor E1 are used to rectify the AC voltage to DC voltage. This rectified DC power supply is fed into the input of the second circuit where LM350 and operational amplifier LM301A are used to control the charging current and voltage of the lead-acid battery. Once the charge is full, transistor Q1 will turn ON and LED L1 will be ON to indicate that the charging has been completed. A heat sink is attached to LM350 to transfer the heat generated from the regulator to the ambient.

This bar-graph LED-battery-level-indicator project is based on the LM3914 monolithic IC of the National Semiconductor that senses the voltage levels of the battery and drives the 10 light-emitting diodes based on the voltage level that is detected. It provides a linear analogue display output and has a pin that can be configured to display the output in moving dot or bar graph. The current driving the LEDs is regulated and programmable, hence limiting resistors are not required. The schematic diagram below shows how the various components are connected. Switch S1 is used to change the display type from moving dot to bar graph type. When S1 is ON, the display type is bar graph, but when it is OFF, the display changes to the moving dot type. R3 is used to set the lower limit of the display. Use a variable DC power supply and set the VBAT to 10,5 V. Adjust VR1 until the LED L1 turns ON. Next, set the VBAT to 15 V; adjust VR2 until all the LEDs turn ON (when S1 is ON).



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COMPONENT LIST		
R1 varistor 14 mm	B1 5 A diode bridge	
R2 500 ohm, 5 W	C1 6 800 uF 35 V electrolytic capacitor	
R3, R6 15 K ¼ W	C2 0,1 uF ceramic 104	
R4 230 ohm ¼ W	C3 1 nF ceramic 102	
R5 1k	C4 1 uF electrolytic 25 volt	
R7 0,2 ohm, 5 W	D1 1N 4148 diode	
R8 3k3 ¼ W	IC1 LM350 16 volt positive voltage regulator	
J1 mains supply	IC2 LM301 H operational amplifier	
J2 12 V connector for battery/battery clamps	S1 On/Off switch for mains voltage	
F1 500 mA fast-blow fuse	S2 push-to-make switch	
TR1 240 V–16 V transformer 3 A (+/-50 VA)	LED 1 red LED 5 mm	
R9 1k2 ¼ W 5%	IC 3 LM3914 N bar-graph display driver	
R10 4k7 ¼ W 5%	C1 10 µF 25 volt electrolytic capacitor	
R11 5k potentiometer	S1 SPST toggle switch	
LED 1–10 LED – red, amber, green		
R12 5k potentiometer		

NOTE: All circuits MUST include an ON/OFF switch with an ON indicator and fuse protection.

7. CONCLUSION

On completion of the practical assessment task, learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.